DIGITAL DESIGN WITH VHDL - 2024/5

Module code: EEE3027

Module Overview

This module provides knowledge about advanced digital circuit design and the hardware description language VHDL. The practical part of the course is concerned with FPGA implementation, using modern CAD tools and FPGA prototyping boards. This module builds on from many Electronic Engineering modules at undergraduate level in the topics of Circuit Design and Processor design such EEE2045 Electrical Science II and will lead on to EEEM059 Space Avionics

Module provider

Computer Science and Electronic Eng

Module Leader

BRIDGES Christopher (Maths & Phys)

Number of Credits: 15

ECTS Credits: 7.5

Framework: FHEQ Level 6

Module cap (Maximum number of students): 50

Overall student workload

Independent Learning Hours: 90

Lecture Hours: 22

Laboratory Hours: 22

Guided Learning: 6

Captured Content: 11

Module Availability

Semester 2

Prerequisites / Co-requisites

EEE2045 – Engineering Science II EEE2048 – Computer Algorithms and Architecture or equivalent digital electronic engineering learning or experience

Module content

Indicative content includes the following.

Introduction. The evolution of VLSI circuits. The role of computer-aided design automation.

Hardware Description Languages. Basics of VHDL. Domains and levels of modeling. System specification: Design units. Signals. Behavioural Modelings. Structural Modelings. Hierarchical modeling concepts. Components of a simulation. Testing a design with a Testbench. Lexical elements. Operators. Syntax descriptions – EBNF. Types. Assignments. Processes. Configurations. VHDL synthesis. Examples of VHDL code.

Combinational logic design with VHDL. Decoders. Encoders. Three-state devices. multiplexers. Exclusive-OR gates and Parity Circuits. Comparators. Adders, Subtractors, and ALUs. Combinational multipliers. With Examples.

Sequential-circuit design with VHDL. Latches and flip-flops. Clocked synchronous state-machine design. Feedback sequential-circuit design. Counters. Shift registers. With Examples.

ASIC Design Methodologies and CAD Tools. Design automation and classes of design tools. Implementation approaches. Field-programmable gate arrays. Intellectual property cores. System-on-a-chip. Pipelining.

Practical Work: The lecture course is accompanied by a set of laboratory exercises on digital design using the hardware description language VHDL. The laboratory work covers all stages of the FPGA design process and involves hands-on exposure to the CAD tools such as Xilinx ISE and a prototyping board (containing a Xilinx Spartan-6 FPGA).

The practical component is used as a project-driven learning vehicle in the course. The students learn and discover new knowledge by carrying out the design assignments. Being given the general principles of VHDL in lectures, they learn further details about the language and the design tools through hands-on experience being guided by computer-aided learning materials, design tutorials and laboratory supervision.

Assessment pattern

Assessment type	Unit of assessment	Weighting
Coursework	ASSIGNMENT 1	20
Coursework	ASSIGNMENT 2	20
Examination	2 HR INVIGILATED EXAM	60

Alternative Assessment

N/A

Assessment Strategy

The assessment strategy for this module is designed to provide students with the opportunity to demonstrate their developed understanding and learning of digital design techniques using VHDL.

The assessments are designed to support the lectures on design principles as well as provide the hands on knowledge required to perform practical VHDL tasks. The two assignments each require a report in which students must concisely describe how the VHDL-code works, and how it is successfully implemented on an FPGA device. It will assess the student's ability to debug, compile, and implement a full design with only guided support from supervisors.

Thus, the summative assessment for this module consists of the following:

- Assignment 1 involves writing, debugging, expanding and simulating of VHDL designs. 10 Pages due Tuesday, Week 6
- Assignment 2 which involves a further VHDL design which is then implemented and tested on the real FPGA hardware. 10 Pages due Tuesday Week 10.
- Final exam that assesses design FPGA and ASIC concepts, methodologies and implementation considerations developed within the module.

Any deadline given here is indicative. For confirmation of exact date and time, please check the Departmental assessment calendar issued to you.

Formative assessment and feedback

For the module, students will receive formative assessment and feedback in the following ways.

- During lectures and by question and answer sessions
- During tutorials/tutorial classes
- During supervised software and hardware laboratory sessions
- Via the marking of written assignments.

Module aims

- Develop understanding of digital circuit design using the VHDL hardware description language .
- Give insight into typical FPGA design implementation concepts and the approaches for application-specific integrated circuit (ASIC).
- Provide hands-on design experience with the Xilinx FPGA simulation, implementation and analysis tools.
- The module also aims to provide opportunities for students to learn about the Surrey Pillars listed below.

Learning outcomes

		Attributes Developed	
Ref			
001	Explain the principles of advanced digital circuit design	KC	C1, C2
002	Describe state-of-the-art ASIC/FPGA design methodologies via an extended essay	KCPT	C3, C16, C17
003	Build FPGA designs using the hardware description language VHDL	KCPT	C5, C6
004	Operate, debug and analyse IP core designs in modern VHDL software tool-chains	KCPT	C4, C6, C12

Attributes Developed

C - Cognitive/analytical

K - Subject knowledge

T - Transferable skills

P - Professional/Practical skills

Methods of Teaching / Learning

On successful completion of this module, students will be able to:

- Explain the principles of advanced digital circuit design
- Describe state-of-the-art ASIC/FPGA design methodologies
- Build FPGA designs using the hardware description language VHDL
- Operate, debug and analyse IP core designs in modern VHDL software tool-chains

Learning and teaching methods include the following.

- Captured content to cover Digital Design Fundamentals
- VHDL Coding Labs with access to key software and hardware tools to develop VHDL skills
- One-to-one Check-ins for opportunities on Lectures and Student Feedback
- Plus other learning material vis SurreyLearn (videos, tutorials, past papers, further study links)

Indicated Lecture Hours (which may also include seminars, tutorials, workshops and other contact time) are approximate and may include in-class tests where one or more of these are an assessment on the module. In-class tests are scheduled/organised separately to taught content and will be published on to student personal timetables, where they apply to taken modules, as soon as they are finalised by central administration. This will usually be after the initial publication of the teaching timetable for the relevant semester.

Reading list

https://readinglists.surrey.ac.uk
Upon accessing the reading list, please search for the module using the module code: EEE3027

Other information

This module has a capped number and may not be available exchange students. Please check with the International Engagement Office email: ieo.incoming@surrey.ac.uk

This module builds on from many Electronic Engineering modules at undergraduate level in the topics of Circuit Design and Processor design.

University Pillars

- Sustainability – This module discusses the trade-off between: power, area and speed towards efficient digital circuits. This is also tested in assessment.
- Digital Capabilities – This entire module is focussed on industry relevant and highly transferable digital skills in VHDL/FPGAs.
- Employability – This VHDL module is critical for the EEE sector in practical and highly wanted real-world skills. Such practical skills ensure employability.

Programmes this module appears in

Programme	Semester	Classification	Qualifying conditions
Electronic Engineering BEng (Hons)	2	Optional	A weighted aggregate mark of 40% is required to pass the module
Electronic Engineering MEng	2	Optional	A weighted aggregate mark of 40% is required to pass the module
Electronic Engineering MSc	2	Optional	A weighted aggregate mark of 40% is required to pass the module
Electronic Engineering with Computer Systems BEng (Hons)	2	Optional	A weighted aggregate mark of 40% is required to pass the module
Electronic Engineering with Computer Systems MEng	2	Optional	A weighted aggregate mark of 40% is required to pass the module
Electronic Engineering with Nanotechnology BEng (Hons)	2	Optional	A weighted aggregate mark of 40% is required to pass the module
Electronic Engineering with Nanotechnology MEng	2	Optional	A weighted aggregate mark of 40% is required to pass the module
Electronic Engineering with Space Systems BEng (Hons)	2	Optional	A weighted aggregate mark of 40% is required to pass the module
Electronic Engineering with Space Systems MEng	2	Optional	A weighted aggregate mark of 40% is required to pass the module